AMENDMENTS TO THE SPECIFICATION

Please amend the specification on page 4, beginning at line 4, as follows:

Therefore, an object of the present invention is to provide an FDTS/DF (Fixed-Delay Tree Search with Decision Feedback equalizer using an absolute value calculation that is capable of reducing the number of gates, improve a calculation speed and reducing the size of a chip.

Please amend the specification on page 6, beginning at line 21, as follows:

That is, when the sampled signal is inputted to the feed-forward ~~finger~~ filter 310, the difference between the feed-forward filtered signal and the feed-back filtered signal is inputted to the detector 330 (at this time, the output of the feed-back filter 320 is a value calculated with the output of the detector 330 outputted prior to one sampling time), and the output signal of the detector 330 is inputted to the feed-back filter 320. Thereafter, the final output of the detector 330 is restored as a data.

Please amend the specification on page 7, beginning at line 5, as follows:

As shown in Figure [[2]] 3, the detector 330 includes branch metric calculating units 410, 420 and 430 obtaining an error between a signal subtracted by the subtractor 340 and a reference signal; an adding unit 460 delaying values calculated by the branch metric calculating units 410, 420 and 430 as deep as τ and adding them; a path metric memory unit 470 storing the added value; a minimum value calculating unit 480 computing a minimum value of the stored value; and a comparator 490 comparing the minimum values and outputting the smallest value.

Please amend the specification on page 7, beginning at line 22, as follows:

The adding unit 460 includes adders 530 and 540 respectively adding the value outputted from the demultiplexer 520 and the path metric prior to the one period of sampling time.